OIPE
MAY 15 2006
PATENT & TRADEMARK OFFICE
1AP22

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Michael G. Kelly
Serial No. : 10/820,484
Filed : April 8, 2004
Title : THERMAL DISSIPATION IN INTEGRATED CIRCUIT SYSTEMS

Art Unit : 2826
Examiner : Andujar, Leonardo

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

I. Real Party in Interest

The real party in interest is Avago Technologies General IP (Singapore) Pte. Ltd. (Company Registration No. 200512430D), a company incorporated under the laws of Singapore whose registered office is at 8 Cross Street, #11-00 PWC Building, Singapore 048424.

II. Related Appeals and Interferences

Appellant is not aware of any related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-21 are pending.

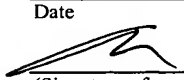
Appellant appeals all rejections of the claims 1-21.

05/16/2006 SHASSEN1 00000061 503718 10820484
01 FC:1402 500.00 DA

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commission for Patents, PO Box 1450, Alexandria, VA 22313-1450 on:

May 9, 2006
Date



(Signature of person mailing papers)

Edouard Garcia
(Typed or printed name of person mailing papers)

IV. Status of Amendments

The Amendment that was filed on November 3, 2005, has been entered and acted upon by the Examiner.

No amendments were filed after the final Office action dated January 30, 2006.

V. Summary of Claimed Subject Matter

The invention claimed in independent claim 1 is an integrated circuit system that includes a die that incorporates an integrated circuit and has a top side and a bottom side. The top side of the die supports an electrical signal communication metallization and a top side thermal dissipation metallization. The bottom side of the die supports a bottom side thermal dissipation metallization.

In embodiments in accordance with the invention defined in claim 1, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization provide high thermal conductivity paths for heat emanating from the integrated circuit die and robust attachments to an integrated circuit package in which the die may be mounted. In this way, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization provide an effective way to remove heat from the integrated circuit die and maintain the temperature of the integrated circuit die within a reliable temperature range, while increasing the mechanical stability of the integrated circuit die and increasing the overall robustness of the final integrated circuit package in which the die may be mounted. In addition, the top side thermal dissipation metallization and the bottom side thermal dissipation metallization may be formed using substrate-scale (e.g., wafer-scale) processing, thereby increasing processing efficiency and allowing the integrated circuit die to be packaged using standard automatic metallurgical bonding equipment.

The specification defines the term "die" as a substrate (usually part of a larger substrate) that contains an integrated circuit" (see page 3, lines 23-24 of the specification). The specification defines the term "metallization" as a "single-layer metal film or a multi-layer metal film formed in or on an integrated circuit" (page 4, lines 3-4).

FIGS. 1A and 1B show an embodiment of a die 10 that incorporates an integrated circuit 12 that constitutes an integrated circuit system in accordance with the invention

defined in independent claim 1. The die 10 has a top side 14 that supports an electrical signal communication metallization 18 and a top side thermal dissipation metallization 20. The top side thermal dissipation metallization 20 defines a thermal contact area on the top side 14 of die 10 that provides a high thermal conductivity path from the die 10 to, for example, a heat spreader of a package into which die 10 will be mounted (see page 4, lines 9-12). The die 10 also has a bottom side 16 that supports a bottom side thermal metallization 17 (see page 4, lines 19-20 of the specification). The bottom side thermal metallization 17 defines a thermal contact area on the bottom side 16 of the die 10 that provides a high thermal conductivity path from the die 10 to, for example, a heat spreader of a package into which die 10 will be mounted (see page 4, lines 20-23).

FIGS. 3, 4A, and 4B show an embodiment of a method of making an integrated circuit system in accordance with the invention defined in independent claim 15. In accordance with this inventive method, multiple die regions 10 are formed on a top side of a substrate 50 (e.g., a semiconductor wafer) (block 52; see page 6,lines 30-32 of the specification). The die regions 10 that are formed on substrate 50 are separated from one another by street areas 54. Each die region 10 has an electrical signal communication metallization 18 and a top side thermal dissipation metallization 20, as described in detail above. A bottom side thermal dissipation metallization 17 is formed on a bottom side of the substrate 50 for each die region (block 56; see page 7, lines 2-4). The bottom side thermal dissipation metallization 17 may be formed as a uniform layer or layers of metal that are deposited onto the bottom side of the substrate 50, as shown in FIG. 4B. Alternatively, the bottom side thermal dissipation metallization 17 may be patterned using, for example, photolithographic processing techniques. The die regions 10 are singulated to form respective integrated circuit dice (block 58; see page 7, lines 8 and 9 of the specification).

As shown in FIG. 1A, the bonding elements of the electrical signal communication metallization 18 are disposed on the top side 14 of die 10 in a peripheral region 22 in accordance with the aspect of the invention defined in claims 3 and 6 (see page 4, lines 25-27 of the specification). The top side thermal dissipation metallization 20 is disposed on the top side of die 10 within a central region 28 surrounded by the peripheral region 22 in accordance with the aspect of the invention defined in claims 4 and 5 (see page 4, lines 31-33 of the specification).

FIGS. 5A and 5B show an embodiment of an integrated circuit die 60 that includes a top side thermal dissipation metallization 62 that has an array of through-holes 64 in accordance with the aspect of the invention defined in claims 8 and 9. These through-holes help to reduce stress buildup in the integrated circuit die 60 (see page 7, lines 18-21).

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1-9, 15-17, and 21 stand rejected under 35 U.S.C. § 103(a) over White (U.S. 5,665,655) in view of Dias (U.S. 6,812,548).

B. Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo (U.S. 6,717,267).

C. Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang (U.S. 5,977,626).

D. Claim 14 stands rejected under 35 U.S.C. § 103(a) over White in view of White in view of Dias, Kunikiyo, and Khan (U.S. 6,853,070).

E. Claim 18 stands rejected under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo.

F. Claims 19 and 20 stand rejected under 35 U.S.C. § 103(a) over White in view of White in view of Dias, Kunikiyo, and Wang

VII. Argument

A. Rejection under 35 U.S.C. § 103(a) over White (U.S. 5,665,655) in view of Dias (U.S. 6,812,548)

The Examiner has rejected claims 1-9, 15-17, and 21 under 35 U.S.C. § 103(a) over White (U.S. 5,665,655) in view of Dias (U.S. 6,812,548).

1. Overview of White's disclosure

In FIG. 25, white discloses a wafer substrate 1 that has active device regions 2, each of which includes at least one electronic element (see col. 5, lines 29-35). On top of the

active device regions 2 are three dielectric layers 3, 36, 47 (see col. 5, line 37 and col. 7, line 3). The dielectric layers 3, 36, 47 include vias containing respective tungsten contacts 6, 38, 44 (see col. 5, line 53 and col. 7, line 4). Interleaved with the dielectric layers 3, 36, 47 are three patterned metal interconnects 9, 39, 46 (see col. 5, line 63, col. 7, line 5). A final passivation layer 48 is formed both over the top dielectric layer 47 and over the top interconnect 46 (see col. 7, lines 5-7).

Etched through the dielectric layers 3, 36, 47 are a pair of grooves 50, 52 that define a dicing area 10 and also function as crack stops that prevent the propagation of microcracks through the dielectric layers 3, 36, 47 (see col. 1, line 56 - col. 2, line 12; col. 5, lines 43-49; col. 6, lines 4-19; col. 7, lines 7-10 and 38-50).

The wafer substrate 1 shown in FIG. 25 is diced through the dicing area 10 between the grooves 50, 52 to form individual dice as shown in FIG. 8 (see col. 6, lines 12-19).

2. Overview of Dias' disclosure

Dias discloses a microelectronic die that has an active surface, a back surface, and a trench sidewall extending from the back surface that is formed prior to backside metallization and dicing (see abstract; col. 1, lines 8-13; col. 3, lines 48-57). The formation of the trench prior to backside metallization "greatly reduces or eliminates delamination between the backside metallization and a thermal interface material subsequently applied to form a thermal contact between the microelectronic die and a heat dissipation device (col. 3, lines 53-57).

In FIG. 3, Dias shows a microelectronic device wafer 100 that includes an active surface 104 that contains microelectronic device circuitry (not shown). An interconnection layer 108, which is on the active surface 104, provides routes for electrical communication between integrated circuit components within the integrated circuits (col. 3, lines 65-67). The interconnection layer 108 consists of alternating layers 112 of dielectric material and layers of patterned electrically conductive material (see col. 4, lines 4-12).

The microelectronic device wafer 100 also includes a back surface 106. A trench 122 is formed in the back surface 106. Subsequently, a backside metallization layer 128 is formed on the back surface 106.

In FIG. 6, Dias shows a microelectronic die 144 that is segmented from the microelectronic device wafer 100. The microelectronic die 144 is attached to a substrate 146 by solder balls 148, which extend between the interconnection layer 108 and the substrate 146 (see col. 5, lines 37-42). A heat dissipation device 152 is attached to the backside metallization layer 128 by a thermal interface material 154 (see col. 5, lines 42-44).

3. Independent claim 1

a. The invention defined by claim 1

Claim 1 recites:

> 1. An integrated circuit system, comprising:
>
> a die incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization, and the bottom side supporting a bottom side thermal dissipation metallization.

b. The Examiner's position regarding claim 1

In his rejection of independent claim 1, the Examiner has stated that FIG. 25 of White shows "an integrated circuit system, comprising: a die 1 incorporating an integrated circuit 2 and having a top side and a bottom side, the top side supporting an electrical signal metallization 6 and a top side thermal dissipation metallization 9 ... " (see ¶ 4 on page 2 of the final Office action). That is, the Examiner has taken the position that:

- the wafer substrate 1 shown in FIG. 25 corresponds to the die recited in claim 1,
- the active device regions 2 shown in FIG. 25 correspond to the integrated circuit recited in claim 1,
- the tungsten contact 6 shown in FIG. 25 corresponds to the electrical signal metallization recited in claim 1, and
- the metal interconnect 9 shown in FIG. 25 corresponds to the top side thermal dissipation metallization.

The Examiner has acknowledged that White does not teach or suggest that the backside of the wafer substrate supports a bottom side thermal metallization (see ¶ on page 2 of the final Office action). In spite of this failure of White's disclosure, the Examiner has concluded that (see ¶ 4 on pages 2-3 of the final Office action):

> Nevertheless, Dias (e.g., FIG. 5) shows a die 102 including a bottom side supporting a bottom side thermal dissipation metallization layer (e.g., gold) 128. This type of embodiment facilitates the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e., stick to) semiconductor wafers (col. 2/lls. 1-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a bottom side thermal dissipation metallization layer in the back surface of the die disclosed by White to facilitate the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e., stick to) semiconductor wafers as taught by Dias.

c. Appellant's rebuttal regarding claim 1

The Examiner's rejection of claim 1 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn for the following reasons.

i. White does not disclose a die having a top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization

Contrary to the Examiner's statement in § A.3.b above, the metal interconnect 9 is not a "thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term.

As shown in FIG. 25, the metal interconnect 9 is part of an electrical signal interconnection system that includes interconnects 9, 39, 46 and contacts 6, 38, 44. The metal interconnect 9 is a buried electrical interconnect that is connected to the underlying active region 2 by the tungsten contact 6 (see, e.g., FIG. 25, col. 5, line 63, and col. 10, line, 12).

One skilled in the art at the time the invention was made would not have considered the electrical interconnect 9 to be a "thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term. In particular, the electrical interconnect 9 is buried under dielectric layers that would interfere with heat dissipation due to their poor heat conduction properties. As a result, there is no way for the heat to readily dissipate away from the integrated circuit, as one skilled in the art would expect from a "thermal dissipation metallization." In addition, the reasonably expected dimensions of the buried electrical interconnect 9 would not be sufficient to produce any appreciable thermal dissipation in the dice disclosed in White. The Examiner has not identified any element in White's disclosure that one skilled in the art reasonably would have considered to be "a thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term.

In apparent response to the Appellant's point that the interconnect 9 is a buried layer, the Examiner has stated that "White's figure 25 clearly shows that the element 9 is atop the thermal dissipation metallization 6" (¶ 34 on page 11 of the final Office action). This statement, however, is inconsistent with the Examiner's assertion that element 6 corresponds to the electrical signal metallization recited in claim 1. Moreover, this statement does not address the point that interconnect 9 is not a "thermal dissipation metallization" in accordance with the ordinary and accustomed meaning of the term.

ii. Dias does not make-up for the failure of White to disclose a die having a top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization

Dias does not make-up for the failure of White to teach or suggest a thermal dissipation metallization that is supported by a top side of a die of an integrated circuit system, as recited in claim 1.

Dias discloses that the top side of the die corresponds to the topmost one of the alternating layers 112 of dielectric material and patterned electrically conducting material (see col. 4, lines 4-12). One skilled in the art at the time the invention was made would not have expected the patterned electrical interconnects disclosed in Dias to have dimensions that are sufficient to produce any appreciable thermal dissipation in the integrated circuit system dice disclosed in Dias for the reasons explained above in connection with White's disclosure. Therefore, one skilled in the art at the time the invention was made would not have had any

reasonable basis to believe that Dias' die includes a thermal dissipation metallization that is supported by a top side of a die of an integrated circuit system, as recited in claim 1.

Thus, neither White nor Dias teaches or suggests an integrated circuit system that includes a top side thermal dissipation metallization supported by a top side of a die as recited in claim 1. Therefore, the combination of White and Dias cannot possibly teach or suggest the invention defined by independent claim 1. For at least these reasons, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

iii. The Examiner's rejection of claim 1 relies on an impermissible combination of the teachings of White and Dias

The Examiner has stated that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a bottom side thermal dissipation metallization layer in the back surface of the die disclosed in White to facilitate the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interface materials do not wet (i.e., stick to) semiconductor wafers as taught by Dias."

The Examiner, however, has not explained why one skill in the art would have been motivated to attach a heat spreader to the back side of White's die in the first place. Indeed, assuming for the purpose of argument only that the Examiner's factually incorrect assertion that the buried interconnect 9 in White's die is a top side thermal dissipation metallization, what would have motivated one skilled in the art at the time the invention was made to attach a second thermal dissipation metallization to the back side of White's die? In ¶ 35 on page 11 of the final Office action, the Examiner has stated that:

> In this case, this type of embodiment facilitates the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e., stick to) semiconductors wafers (sol. 2/lls. 1-14). As it is well known in the art heat sink are used to improve the heat dissipation of the IC die in order to avoid problems associated with high temperatures within the IC such as speed problems. In addition to heat dissipation through the top side metallization layers bottom side heat dissipation would greatly improve the overall heat dissipation.

However, White does not teach or suggest anything about the desirability of attaching heat spreaders to the top or bottom sides of a die, and Dias only teaches attaching a single heat spreader to the back side of an integrated circuit die. For this reason, the Examiner's reliance on well-known knowledge in ¶ 35 of the final Office action amounts to no more than the impermissible "obvious to try" rationale for finding obviousness, which is not the proper standard for rejecting a claim (see, e.g., MPEP § 2145.X.B).

For these reasons, it appears that the Examiner improperly has engaged in hindsight reconstruction of the claimed invention, using applicants' disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper *prima facie* case of obviousness and the rejection of claim 1 should be withdrawn for this additional reason.

iv. Conclusion

For the reasons explained above, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

4. Dependent claims 2-9 and 21

Each of claims 2-9 and 21 incorporates the features of independent claim 1 and therefore is patentable over White in view of Dias for at least the same reasons explained above.

Claims 2-6, 8, 9, and 21 also are patentable over White and Dias for the following additional reasons.

a. Claim 2

Claim 2 recites that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die. The ordinary and accustomed meaning of the term "exposed" is "open to view" or "not shielded or protected" or "not insulated" (Merriam-Webster's Collegiate Dictionary, 10th Ed.). The specification

uses the term "bonding elements" to refer to elements of the electrical signal communication metallization 18 that define the electrical contact areas on the die 10 for electrical wires, lines or traces carrying electrical signals (e.g., input/output signals) between the integrated circuit 12 and one or more external components or devices (see page 4, lines 4-9).

Without pointing to any supporting disclosure in White, the Examiner has stated that "White shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die" (see ¶ 5 on page 3 of the final Office action). In his rejection of claim 1, the Examiner has stated that the contact 6 corresponds to the electrical signal communication metallization. The contact 6, however, does not comprise a plurality of exposed bonding elements on the top side of White's die. Indeed, the contact 6 is a buried tungsten plug that connects the interconnect 9 to the active region 2. Thus, the contact 6 does not comprise a plurality of "bonding elements" nor is it "exposed" in accordance with any reasonable interpretation of the term.

For at least this additional reason, the Examiner's rejection of claim 2 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

b. Claim 3

Claim 3 depends from claim 2 and therefore is patentable over White and Dias for at least the same reasons explained above.

c. Claim 4

Claim 4 depends from claim 3 and therefore is patentable over White and Dias for at least the same reasons explained above.

d. Claim 5

Claim 5 depends from claim 4 and therefore is patentable over White and Dias for at least the same reasons explained above. Claim 5 also is patentable over White and Dias for the following additional reason.

Without pointing to any supporting disclosure in White, the Examiner has stated that "White shows that the topside thermal dissipation metallization is surrounded by the plurality of bonding elements" (see ¶ 8 on page 3 of the final Office action). The ordinary and accustomed meaning of the term "surround" is "to enclose on all sides" (Merriam-Webster's Collegiate Dictionary, 10th Ed.).

As shown clearly in FIG. 25, the interconnect 9 (which the Examiner has stated corresponds to the top side thermal dissipation metallization) extends above and beyond the tungsten contact 6 (which the Examiner has stated comprises the plurality of bonding elements). In addition, the interconnect 9 and the tungsten contact 6 are located at different elevations above the substrate 1. For theses reasons, one skilled in the art at the time the invention was made would not have understood that the tungsten contact 6 "surrounds" the interconnect 9 in accordance with the ordinary and accustomed meaning of the term.

For at least this additional reason, the Examiner's rejection of claim 5 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

e. Claim 6

Claim 6 recites that the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Without pointing to any supporting disclosure in White, the Examiner has stated that "White shows that the electrical signal communication metallization surrounds the topside thermal dissipation metallization" (see ¶ 9 on page 3 of the final Office action). The ordinary and accustomed meaning of the term "surround" is "to enclose on all sides" (Merriam-Webster's Collegiate Dictionary, 10th Ed.).

As shown clearly in FIG. 25, the interconnect 9 (which the Examiner has stated corresponds to the top side thermal dissipation metallization) extends above and beyond the tungsten contact 6 (which the Examiner has stated comprises the plurality of bonding elements). In addition, the interconnect 9 and the tungsten contact 6 are located at different elevations above the substrate 1. For theses reasons, one skilled in the art at the time the invention was made would not have understood that the tungsten contact 6 "surrounds" the interconnect 9 in accordance with the ordinary and accustomed meaning of the term.

For at least this additional reason, the Examiner's rejection of claim 6 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

f. Claim 8

Claim 8 recites that the patterned metal layer comprises at least one through-hole.

The Examiner has stated that the contact 38, which is disposed over the interconnect 9 shown in FIG. 25, corresponds to the through-hole recited in claim 8 (see ¶ 11 on page 3 of the final Office action). The contact 38, however, clearly is not a through-hole, much less is it a through-hole of the interconnect 9. It is noted that the contact 38 is formed in a hole in the dielectric layer 36, but the hole in the dielectric layer 36 is not a through-hole of the interconnect 9.

For at least this additional reason, the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

g. Claim 9

Claim 9 depends from claim 8 and recites that the patterned metal layer comprises an array of through-holes.

The Examiner has stated that the elements 38 and 39, which are disposed over the interconnect 9 shown in FIG. 25, corresponds to the array of through-hole recited in claim 9 (see ¶ 12 on page 4 of the final Office action). As explained above, element 38 is a tungsten contact and element 39 is a patterned interconnect. These elements clearly are not through-holes, much less are they through-holes of the interconnect 9.

For at least this additional reason, the Examiner's rejection of claim 9 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

h. Claim 21

Claim 21 recites that the electrical signal communication metallization is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die.

Without pointing to any supporting disclosure in White, the Examiner has stated that "White shows that the electrical signal communication [metallization] is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die" (see ¶ 13 on page 4 of the final Office action). This statement, however, is incorrect since FIG. 25 clearly shows that the interconnect 9 (which the Examiner has stated corresponds to the top side thermal dissipation metallization) is in direct physical and electrical contact with the tungsten contact 6 (which the Examiner has stated corresponds to the top side thermal dissipation metallization).

For at least this additional reason, the Examiner's rejection of claim 21 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

5. Independent claim 15

Independent claim 15 recites features that essentially track the pertinent features discussed above in connection with independent claim 1 and therefore is patentable over White and Dias for at least the same reasons explained above in connection with independent claim 1.

In addition, independent claim 15 recites "forming on a top side of a substrate multiple die regions each having a top side supporting an exposed electrical signal communication metallization and an exposed top side thermal dissipation metallization."

In his rejection of claim 15, the Examiner has stated that White discloses this feature of claim 15. In particular, the Examiner has stated that the contact 6 corresponds to the "exposed electrical signal communication metallization" and the interconnect 9 corresponds to the "exposed top side thermal dissipation metallization." Contrary to the Examiner's statement, however, FIG. 25 clearly shows that contact 6 and interconnect 9 both are buried under a number of overlying layers. Thus, neither contact 6 nor interconnect 9 is "exposed" in accordance with the ordinary and accustomed meaning of the term (i.e., "open to view" or "not shielded or protected" or "not insulated," Merriam-Webster's Collegiate Dictionary, 10th Ed.).

Dias does not specify whether the topmost one of the interconnect layers 112 is a dielectric material or a patterned electrically conductive material. In accordance with the

knowledge generally available, however, one skilled in the art at the time the invention was made would have understood that the topmost layer of an interconnect layer stack of the type disclosed in Dias would have been a dielectric passivation layer (see, e.g., the passivation layer 48 shown in FIG. 25 of White).

Therefore, neither White nor Dias teaches or suggests "forming on a top side of a substrate multiple die regions each having a top side supporting an exposed electrical signal communication metallization and an exposed top side thermal dissipation metallization." For at least this additional reason, the Examiner's rejection of independent claim 15 under 35 U.S.C. § 103(a) over White and Dias should be withdrawn.

6. Claims 16 and 17

Each of claims 16 and 17 incorporates the features of independent claim 15 and therefore is patentable over White in view of Dias for at least the same reasons explained above.

Claims 16 and 17 also are patentable over White and Dias for the following additional reasons.

a. Claim 16

Claim 16 recites that, in each die region, the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

As explained above in connection with claim 6, FIG. 25 clearly shows that the interconnect 9 (which the Examiner has stated corresponds to the top side thermal dissipation metallization) extends above and beyond the tungsten contact 6 (which the Examiner has stated comprises the plurality of bonding elements). In addition, the interconnect 9 and the tungsten contact 6 are located at different elevations above the substrate 1. For theses reasons, one skilled in the art at the time the invention was made would not have understood that the tungsten contact 6 "surrounds" the interconnect 9 in accordance with the ordinary and accustomed meaning of the term (i.e., "to enclose on all sides," Merriam-Webster's Collegiate Dictionary, 10th Ed.).

For at least this additional reason, the Examiner's rejection of claim 16 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

b. Claim 17

Claim 17 recites that each top side thermal dissipation metallization comprises an exposed metal layer with an array of through-holes.

Without pointing to any supporting disclosure in White, the Examiner has stated that "White teaches that each top side thermal dissipation metallization comprises an exposed metal layer with an array of through-holes" (see ¶ 16 on page 5 of the final Office action). In his rejection of claim 8, the Examiner has stated that the contact 38, which is disposed over the interconnect 9 shown in FIG. 25, corresponds to a through-hole of the top side thermal dissipation metallization (see ¶ 11 on page 3 of the final Office action). The contact 38, however, clearly is not a through-hole, much less is it a through-hole of the interconnect 9 (which the Examiner has stated corresponds to the top side thermal dissipation metallization). It is noted that the contact 38 is formed in a hole in the dielectric layer 36, but the hole in the dielectric layer 36 is not a through-hole of the interconnect 9.

In addition, the interconnect 9 does not comprise an "exposed" metal layer. Indeed, FIG. 25 clearly shows that the interconnect 9 is buried under a number of overlying layers. Thus, the interconnect 9 is not "exposed" in accordance with the ordinary and accustomed meaning of the term (i.e., "open to view" or "not shielded or protected" or "not insulated," Merriam-Webster's Collegiate Dictionary, 10th Ed.).

For at least these additional reasons, the Examiner's rejection of claim 17 under 35 U.S.C. § 103(a) over White in view of Dias should be withdrawn.

B. Rejection under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo (U.S. 6,717,267)

The Examiner has rejected claims 10 and 11 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo (U.S. 6,717,267).

Claim 10 depends from claim 1 and additionally recites that the integrated circuit system includes a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die.

In his rejection of claim 10, the Examiner has stated that Kunikiyo "shows a top heat spreader 32 metallurgically bonded (31) to the top side thermal dissipation metallization of the die (dummy pattern 25a)" (see ¶ 18 on page 5 of the final Office action). Kunikiyo discloses attaching a heat sink 32 to plugs 31 that are formed in a passivation film 30 (see col. 23, lines 1-18). Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plugs 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plugs 31, as recited in claim 10.

For at least these reasons the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo should be withdrawn.

Claim 11 depends from claim 10 and therefore is patentable over White in view of Dias and Kunikiyo for at least the same reasons.

It is noted that Kunikiyo only discloses attaching a single heat spreader to an integrated circuit die.

C. Rejection under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang (U.S. 5,977,626)

The Examiner has rejected claims 12 and 13 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang (U.S. 5,977,626).

Each of claims 12 and 13 incorporates the features of claim 10.

The Examiner has cited Wang for showing "a package having a good efficiency of spreading heat and enhanced EM shielding that includes an electrical interface 28 and a substrate 20 containing a wiring interconnection between the electrical signal communication metallization and the electrical interface" (see ¶ 21 on page 6 of the final Office action). Wang, however, does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. To the contrary, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53).

For at least these reasons the Examiner's rejection of claims 12 and 13 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang should be withdrawn.

It is noted that Wang does not teach or suggest anything about either a top side thermal dissipation metallization or a back side thermal dissipation metallization.

D. Rejection under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Khan (U.S. 6,853,070)

The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Khan (U.S. 6,853,070)..

Claim 14 incorporates the features of claim 10.

Khan does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. To the contrary, Khan teaches that the drop-in heat spreader 202 is attached to the top side of the die 102 using an epoxy 204 (see FIG. 2A and col. 7, lines 29-31). In addition, Khan fails to teach or suggest anything about a top side thermal dissipation metallization.

For at least these reasons the Examiner's rejection of claim 14 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Khan should be withdrawn.

The Examiner's rejection of claim 14 also should be withdrawn for the following additional reasons.

Claim 14 recites that the package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die. The Examiner has stated that "Khan (e.g., fig. 2A) shows a bottom heat spreader 110 bonded to the bottom side thermal dissipation metallization of the die 102." Khan, however, teaches that the heat spreader 110 is attached to the bottom side of the die 102 using an epoxy (see col. 4, lines 60-61). In addition, contrary to the Examiner's assumption, Khan does not teach or suggest that the die 102 includes a bottom side thermal dissipation metallization.

E. Rejection under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo

The Examiner has rejected claim 18 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo.

Claim 18 incorporates the features of independent claim 15.

In his rejection of claim 18, the Examiner has stated that Kunikiyo "shows the step of metallurgically bonding a top heat spreader of the package (e.g., 31) to the top side thermal dissipation metallization of the singulated die (dummy pattern 25a)." Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31, as recited in claim 18.

For at least these reasons the Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) over White in view of Dias and Kunikiyo should be withdrawn.

As noted above, Kunikiyo only discloses attaching a single heat spreader to an integrated circuit die.

F. Rejection under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang

The Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang.

Each of claims 19 and 20 incorporates the features of claim 18.

Wang does not make-up for the failure of White, Dias, and Kunikiyo to teach or suggest the features discussed above in connection with claim 18. To the contrary, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53).

For at least these reasons the Examiner's rejection of claims 19 and 20 under 35 U.S.C. § 103(a) over White in view of Dias, Kunikiyo, and Wang should be withdrawn.

As noted above, Wang does not teach or suggest anything about either a top side thermal dissipation metallization or a back side thermal dissipation metallization.

VIII. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

Date: May 9, 2006

Edouard Garcia
Reg. No. 38,461
Telephone No.: (650) 289-0904

Please direct all correspondence to:

Avago Technologies, Inc.
c/o Klass, Law, O'Meara & Malkin, P.C.
PO Box 1920
Denver, CO 80201-1920

CLAIMS APPENDIX

The claims that are the subject of Appeal are presented below.

Claim 1 (original): An integrated circuit system, comprising:

a die incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization, and the bottom side supporting a bottom side thermal dissipation metallization.

Claim 2 (previously presented): The system of claim 1, wherein the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die.

Claim 3 (previously presented): The system of claim 2, wherein the bonding elements are contained in a peripheral region on the top side of the die.

Claim 4 (previously presented): The system of claim 3, wherein the top side thermal dissipation metallization is contained in a central region on the top side of the die.

Claim 5 (previously presented): The system of claim 4, wherein the top side thermal dissipation metallization is surrounded by the plurality of bonding elements.

Claim 6 (previously presented): The system of claim 1, wherein the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Claim 7 (original): The system of claim 1, wherein the top side thermal dissipation metallization comprises a patterned metal layer.

Claim 8 (original): The system of claim 7, wherein the patterned metal layer comprises at least one through-hole.

Claim 9 (original): The system of claim 8, wherein the patterned metal layer comprises an array of through-holes.

Claim 10 (original): The system of claim 1, further comprising a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die.

Claim 11 (original): The system of claim 10, wherein the integrated circuit is connected electrically to the top side heat spreader by an electrical path extending through the top side thermal dissipation metallization.

Claim 12 (original): The system of claim 10, wherein the package further comprises an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface.

Claim 13 (original): The system of claim 12, wherein the top heat spreader is mounted on the substrate and forms a lid of the package covering the top side of the die.

Claim 14 (original): The system of claim 10, wherein the package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die.

Claim 15 (previously presented): A method of making an integrated circuit system, comprising:

forming on a top side of a substrate multiple die regions each having a top side supporting an exposed electrical signal communication metallization and an exposed top side thermal dissipation metallization;

forming on a bottom side of the substrate an exposed bottom side thermal dissipation metallization for each die region; and

singulating the die regions to form respective integrated circuit dice.

Claim 16 (previously presented): The method of claim 15, wherein, in each die region, the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Claim 17 (previously presented): The method of claim 15, wherein each top side thermal dissipation metallization comprises an exposed metal layer with an array of through-holes.

Claim 18 (original): The method of claim 15, further comprising mounting each singulated die in a respective package having a top heat spreader, wherein mounting a singulated die comprises metallurgically bonding the top heat spreader of a package to the top side thermal dissipation metallization of the singulated die.

Claim 19 (original): The method of claim 18, wherein the package additionally includes a substrate and mounting the singulated die further comprises mounting the package substrate to the bottom side thermal dissipation metallization of the singulated die.

Claim 20 (original): The method of claim 18, wherein the top heat spreader is mounted on the substrate and forms a lid of the package, and further comprising encapsulating the die within the package with an encapsulating material.

Claim 21 (previously presented): The system of claim 1, wherein the electrical signal communication metallization is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 CFR §§ 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner and relied upon by Appellant in the pending appeal. Therefore, no copies are required under 37 CFR § 41.37(c)(1)(ix) in the pending appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any decisions rendered by a court or the Board that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal. Therefore, no copies are required under 37 CFR § 41.37(c)(1)(x) in the pending appeal.

$BAF/1fw

AVAGO TECHNOLOGIES, LTD.
P.O. Box 1920
Denver, Colorado 80201-1920

ATTORNEY DOCKET NO. 10031133-1

OIPE IAP22
MAY 15 2006
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael G. Kelly

Serial No.: 10/820,484 Examiner: Andujar, Leonardo

Filing Date: April 8, 2004 Group Art Unit: 2826

Title: THERMAL DISSIPATION IN INTEGRATED CIRCUIT SYSTEMS

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on March 14, 2006 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-3718** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: May 9, 2006 **OR**

☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile:

Typed Name: Edouard Garcia

Signature:

Respectfully submitted,

Michael G. Kelly

By

Edouard Garcia
Attorney/Agent for Applicant(s)

Reg. No. 38,461

Date: May 9, 2006

Telephone No. (650) 289-0904